SYSTEM FOR ESD PROTECTION WITH EXTRA HEADROOM IN RELATIVELY LOW SUPPLY VOLTAGE INTEGRATED CIRCUITS

ABSTRACT OF THE DISCLOSURE

An ESD protection system providing extra headroom at an integrated circuit (IC) terminal pad. The system includes an ESD protection circuit having one or more first diodes coupled in series between the supply voltage and terminal pad, and a second diode coupled to ground. One or more third diodes are coupled in series between the terminal pad and second diode, and are configured to permit a voltage on the interconnection nodes between the one or more third diodes and second diode different from ground. The one or more third diodes include an n+ on an area of P-substrate. A deep N-well separates the area of P-substrate from a common area of P-substrate, which is coupled to ground. The allowable signal swing at the terminal pad is increased to greater than supply voltage plus 1.4 V. The ESD protection circuit is useful for, among other things, relatively low supply voltage ICs.